



**CYPRESS**  
P E R F O R M

**CY7C1019BN**

**128K x 8 Static RAM**

## Features

- High speed
  - $t_{AA} = 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  options
- Functionally equivalent to CY7C1019

## Functional Description

The CY7C1019BN is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

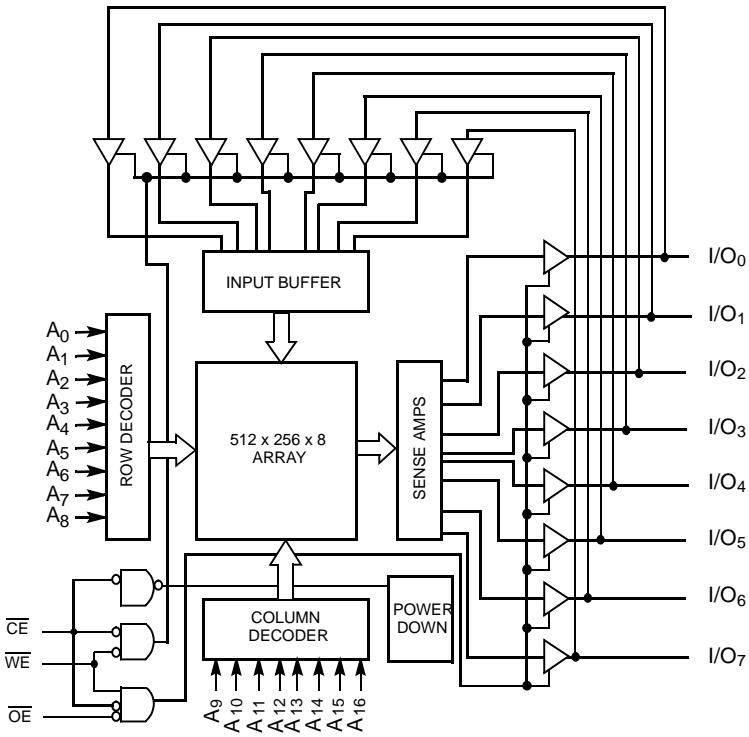
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) are placed in a high-impedance state when the device is deselected ( $\text{CE}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1019BN is available in standard 32-pin TSOP Type II and 400-mil-wide SOJ packages.

## Logic Block Diagram



## Pin Configurations

### SOJ / TSOPII

#### Top View

$\text{A}_0$	1	32	$\text{A}_{16}$
$\text{A}_1$	2	31	$\text{A}_{15}$
$\text{A}_2$	3	30	$\text{A}_{14}$
$\text{A}_3$	4	29	$\text{A}_{13}$
$\overline{\text{CE}}$	5	28	$\overline{\text{OE}}$
$\text{I/O}_0$	6	27	$\text{I/O}_7$
$\text{I/O}_1$	7	26	$\text{I/O}_6$
$\text{V}_{\text{CC}}$	8	25	$\text{V}_{\text{SS}}$
$\text{V}_{\text{SS}}$	9	24	$\text{V}_{\text{CC}}$
$\text{I/O}_2$	10	23	$\text{I/O}_5$
$\text{I/O}_3$	11	22	$\text{I/O}_4$
$\overline{\text{WE}}$	12	21	$\text{A}_{12}$
$\text{A}_4$	13	20	$\text{A}_{11}$
$\text{A}_5$	14	19	$\text{A}_{10}$
$\text{A}_6$	15	18	$\text{A}_9$
$\text{A}_7$	16	17	$\text{A}_8$

**Selection Guide**

	<b>7C1019BN-12</b>	<b>7C1019BN-15</b>	<b>Unit</b>
Maximum Access Time	12	15	ns
Maximum Operating Current	140	130	mA
Maximum Standby Current	10	10	mA
L	1	1	mA

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature with Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage on  $V_{\text{CC}}$  to Relative GND<sup>[1]</sup> ....  $-0.5\text{V}$  to  $+7.0\text{V}$

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> .....  $-0.5\text{V}$  to  $V_{\text{CC}} + 0.5\text{V}$

DC Input Voltage<sup>[1]</sup> .....  $-0.5\text{V}$  to  $V_{\text{CC}} + 0.5\text{V}$

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....  $>2001\text{V}$   
(per MIL-STD-883, Method 3015)

Latch-Up Current .....  $>200\text{ mA}$

**Operating Range**

<b>Range</b>	<b>Ambient Temperature<sup>[2]</sup></b>	<b><math>V_{\text{CC}}</math></b>
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$5\text{V} \pm 10\%$

**Electrical Characteristics** Over the Operating Range

<b>Parameter</b>	<b>Description</b>	<b>Test Conditions</b>	<b>-12</b>		<b>-15</b>		<b>Unit</b>
			<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	
$V_{\text{OH}}$	Output HIGH Voltage	$V_{\text{CC}} = \text{Min.}$ , $I_{\text{OH}} = -4.0\text{ mA}$	2.4		2.4		V
$V_{\text{OL}}$	Output LOW Voltage	$V_{\text{CC}} = \text{Min.}$ , $I_{\text{OL}} = 8.0\text{ mA}$		0.4		0.4	V
$V_{\text{IH}}$	Input HIGH Voltage		2.2	$V_{\text{CC}} + 0.3$	2.2	$V_{\text{CC}} + 0.3$	V
$V_{\text{IL}}$	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
$I_{\text{IX}}$	Input Leakage Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$	-1	+1	-1	+1	$\mu\text{A}$
$I_{\text{OZ}}$	Output Leakage Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$ , Output Disabled	-5	+5	-5	+5	$\mu\text{A}$
$I_{\text{CC}}$	$V_{\text{CC}}$ Operating Supply Current	$V_{\text{CC}} = \text{Max.}$ , $I_{\text{OUT}} = 0\text{ mA}$ , $f = f_{\text{MAX}} = 1/\tau_{\text{RC}}$		140		130	mA
$I_{\text{SB1}}$	Automatic CE Power-Down Current — TTL Inputs	$\text{Max. } V_{\text{CC}}$ , $\text{CE} \geq V_{\text{IH}}$ $V_{\text{IN}} \geq V_{\text{IH}}$ or $V_{\text{IN}} \leq V_{\text{IL}}$ , $f = f_{\text{MAX}}$		40		40	mA
			L		20		
$I_{\text{SB2}}$	Automatic CE Power-Down Current — CMOS Inputs	$\text{Max. } V_{\text{CC}}$ , $\text{CE} \geq V_{\text{CC}} - 0.3\text{V}$ , $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$ , or $V_{\text{IN}} \leq 0.3\text{V}$ , $f = 0$		10		10	mA
			L		1		

**Capacitance<sup>[3]</sup>**

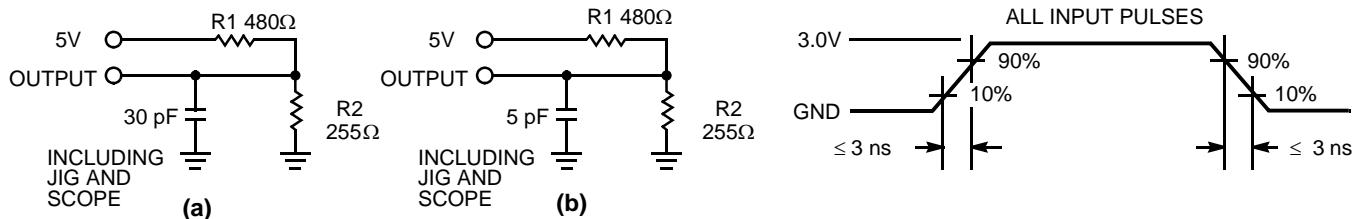
<b>Parameter</b>	<b>Description</b>	<b>Test Conditions</b>	<b>Max.</b>	<b>Unit</b>
$C_{\text{IN}}$	Input Capacitance	$T_A = 25^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{\text{CC}} = 5.0\text{V}$	6	pF
$C_{\text{OUT}}$	Output Capacitance		8	pF

**Notes:**

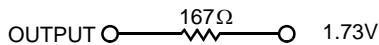
1.  $V_{\text{IL}}$  (min.) =  $-2.0\text{V}$  for pulse durations of less than 20 ns.

2.  $T_A$  is the "Instant On" case temperature.

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT


**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

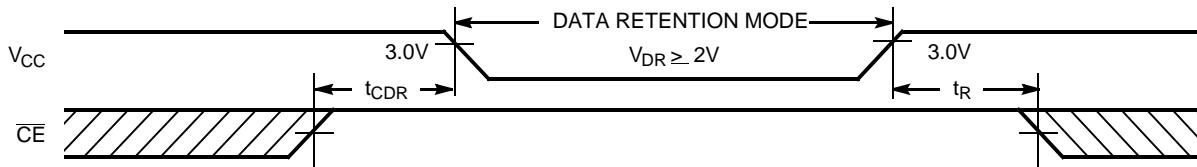
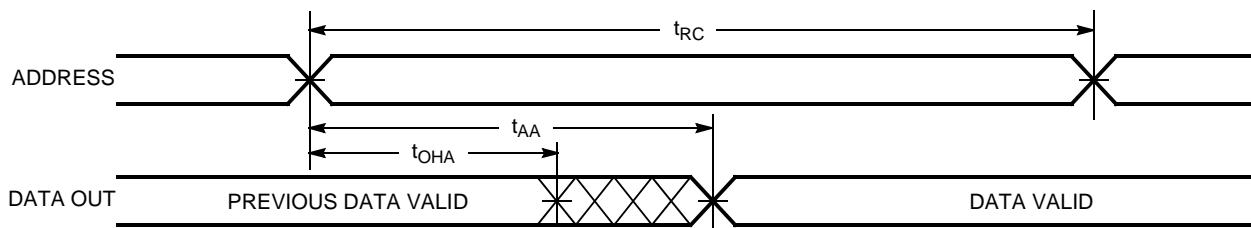
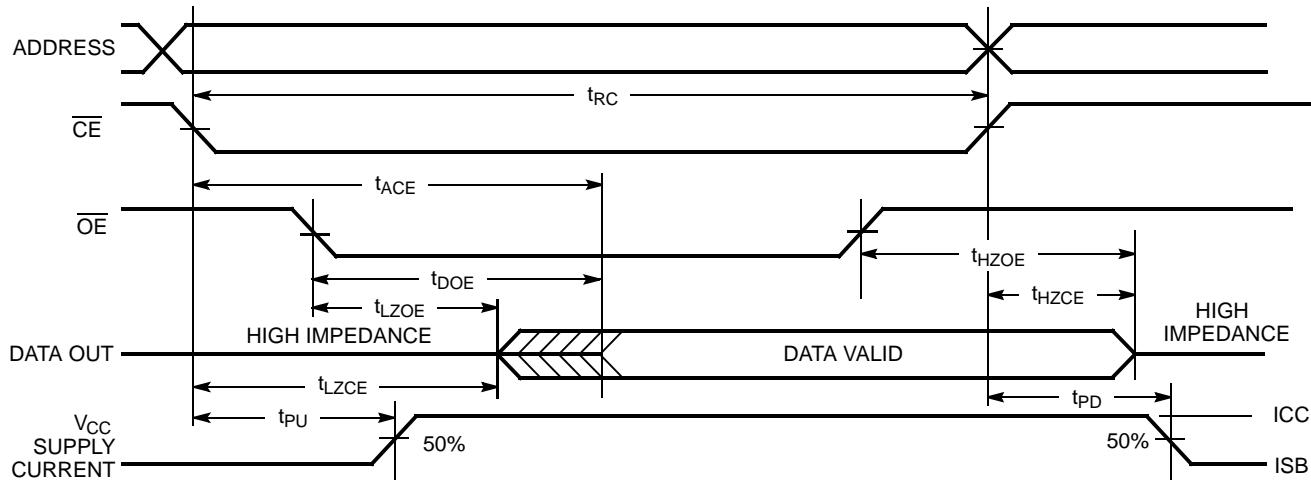
Parameter	Description	-12		-15		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	12		15		ns
$t_{AA}$	Address to Data Valid		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12		15	ns
<b>Write Cycle<sup>[7, 8]</sup></b>						
$t_{WC}$	Write Cycle Time	12		15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	9		10		ns
$t_{AW}$	Address Set-Up to Write End	8		10		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	WE Pulse Width	8		10		ns
$t_{SD}$	Data Set-Up to Write End	6		8		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	WE HIGH to Low Z <sup>[6]</sup>	3		3		ns
$t_{HZWE}$	WE LOW to High Z <sup>[5, 6]</sup>		6		7	ns

**Notes:**

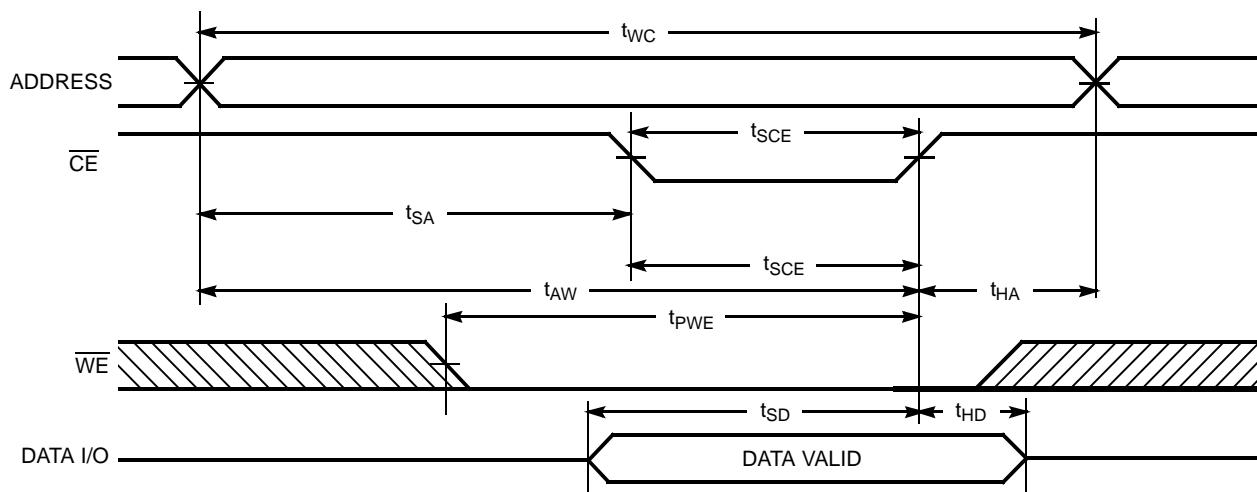
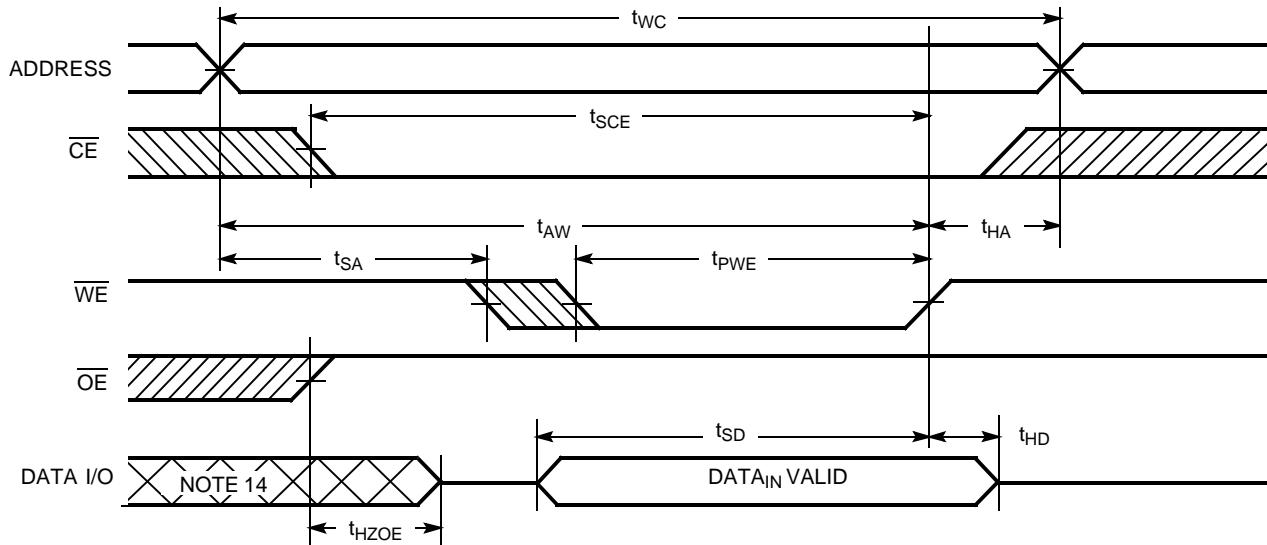
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range (L Version Only)

Parameter	Description	Conditions	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	No input may exceed $V_{CC} + 0.5V$ $V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
$I_{CCDR}$	Data Retention Current			300	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R$	Operation Recovery Time		200		$\mu s$

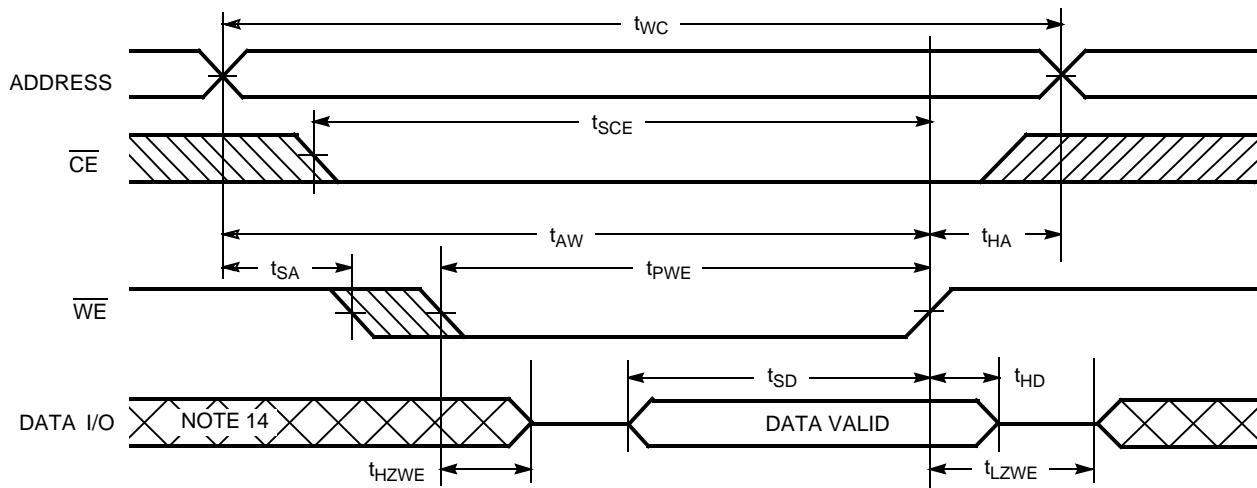
**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[9, 10]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>**

**Notes:**

9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
10.  $\overline{WE}$  is HIGH for read cycle.
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[12, 13]</sup>**

**Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write)<sup>[12, 13]</sup>**

**Notes:**

12. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**

 Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[13]</sup>

**Truth Table**

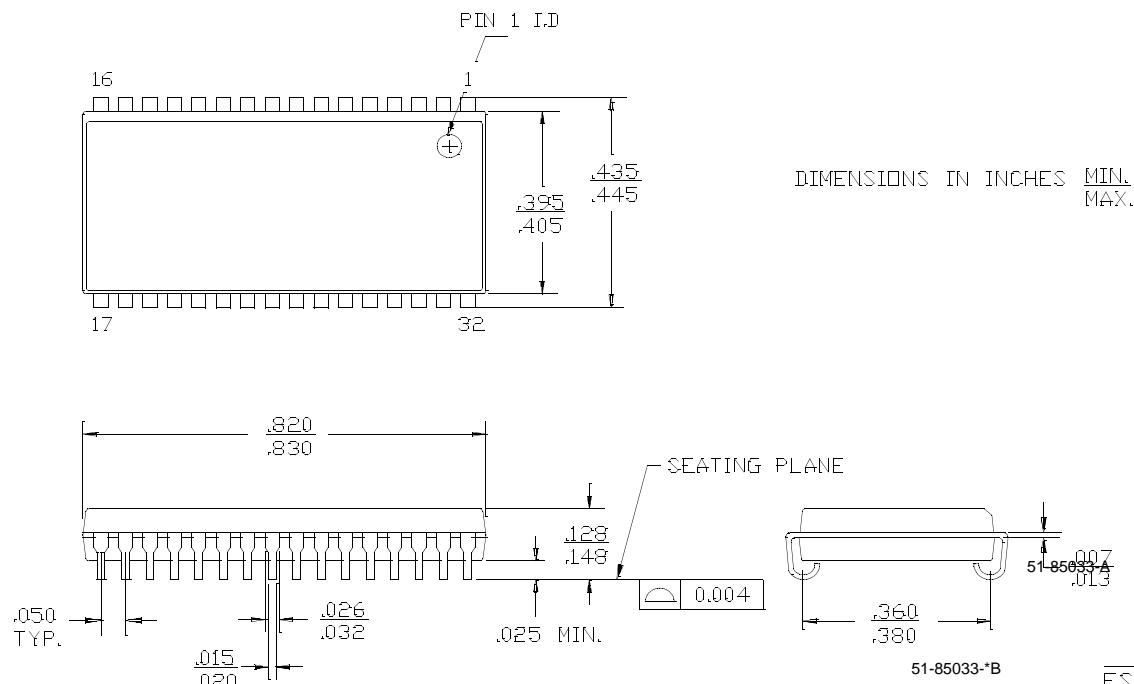
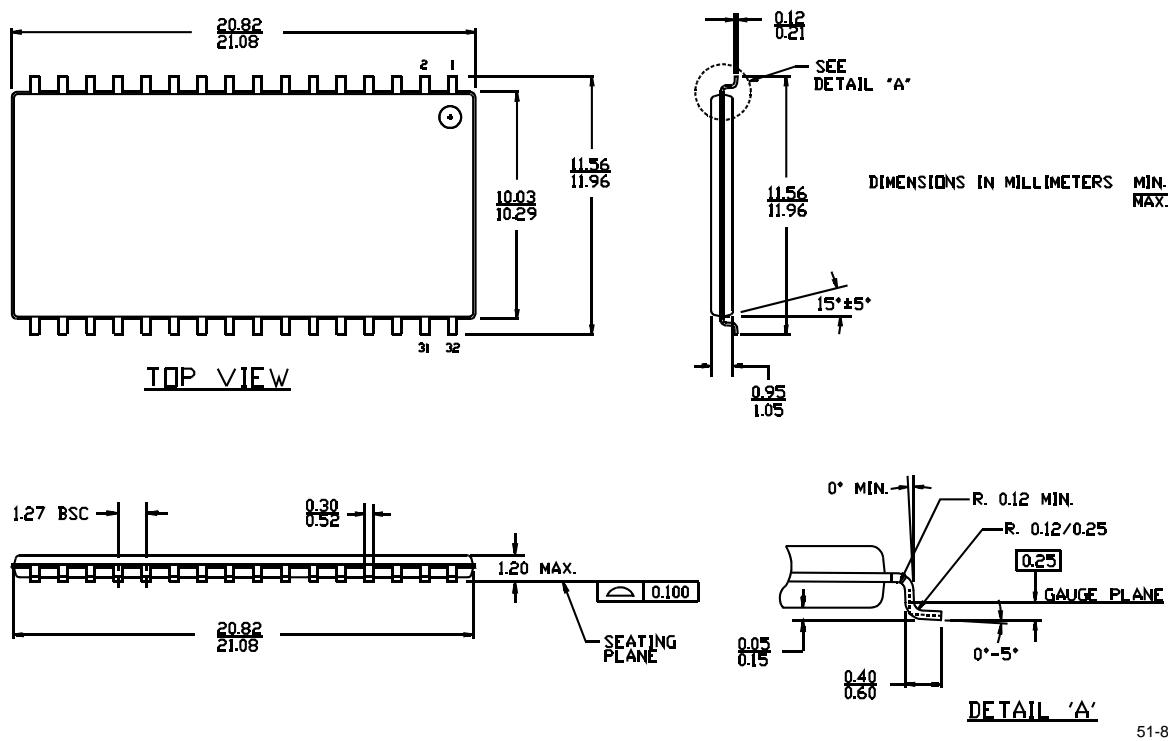
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\text{I/O}_0\text{--}\text{I/O}_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1019BN-12VC	51-85033	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019BN-12ZC	51-85095	32-Lead TSOP Type II	
	CY7C1019BN-12ZXC	51-85095	32-Lead TSOP Type II (Pb-free)	
15	CY7C1019BN-15VC	51-85033	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019BN-15ZXC	51-85095	32-Lead TSOP Type II (Pb-free)	

Please contact local sales representative regarding availability of these parts

## Package Diagrams

**32-pin (400-mil) Molded SOJ (51-85033)**

**32-pin TSOP II (51-85095)**


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## Document History Page

<b>Document Title: CY7C1019BN 128K x 8 Static RAM</b> <b>Document Number: 001-06425</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	423847	See ECN	NXR	New Data Sheet